FIG. 1

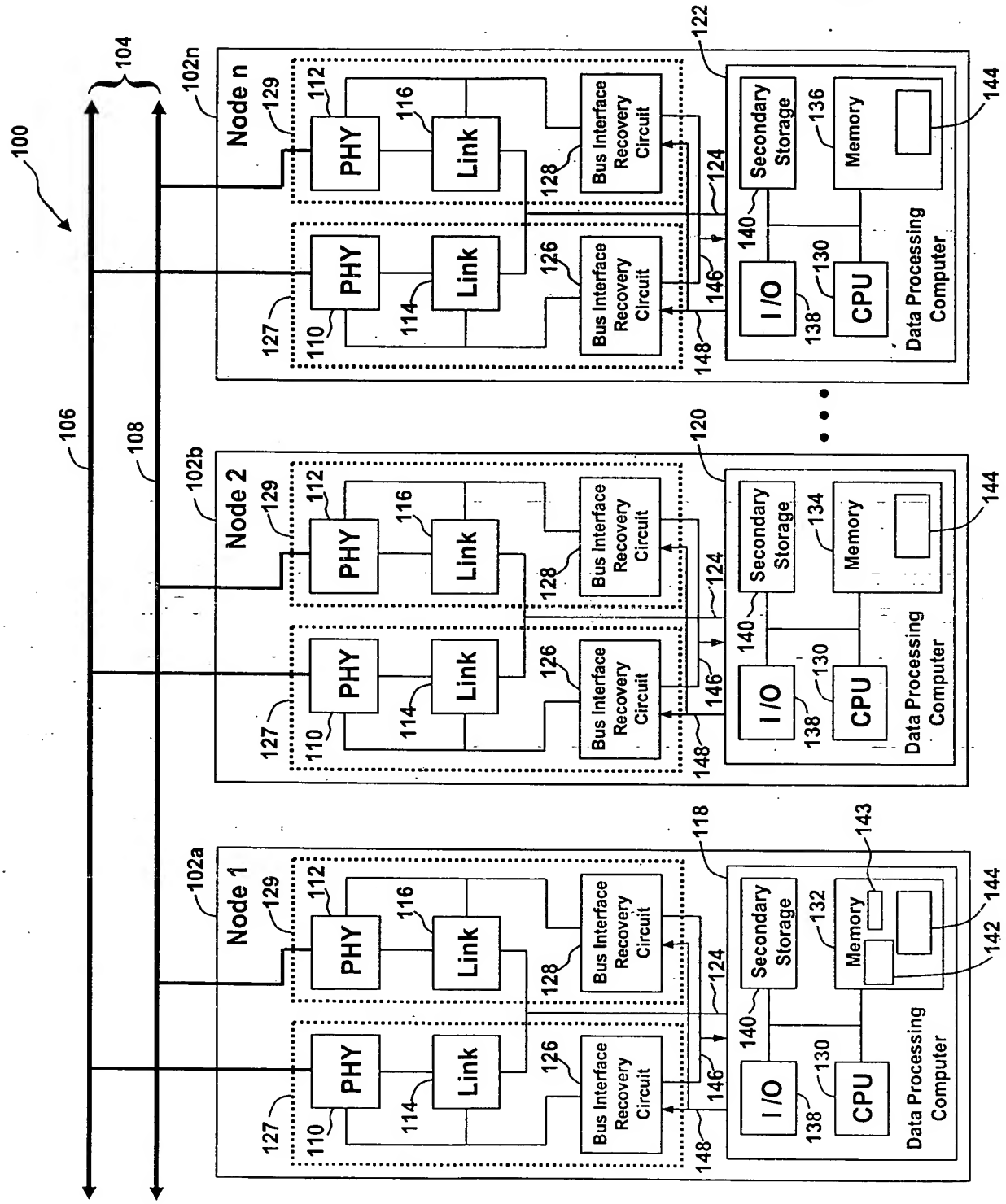

100
104
106
108
102a
Node 1
102b
Node 2
102n
Node n
129
112
PHY
116
Link
128
Bus Interface Recovery Circuit
127
110
114
126
124
118
120
122
140
Secondary Storage
132
134
136
Memory
143
142
144
138
I /O
130
CPU
Data Processing Computer
146
148

FIG. 2

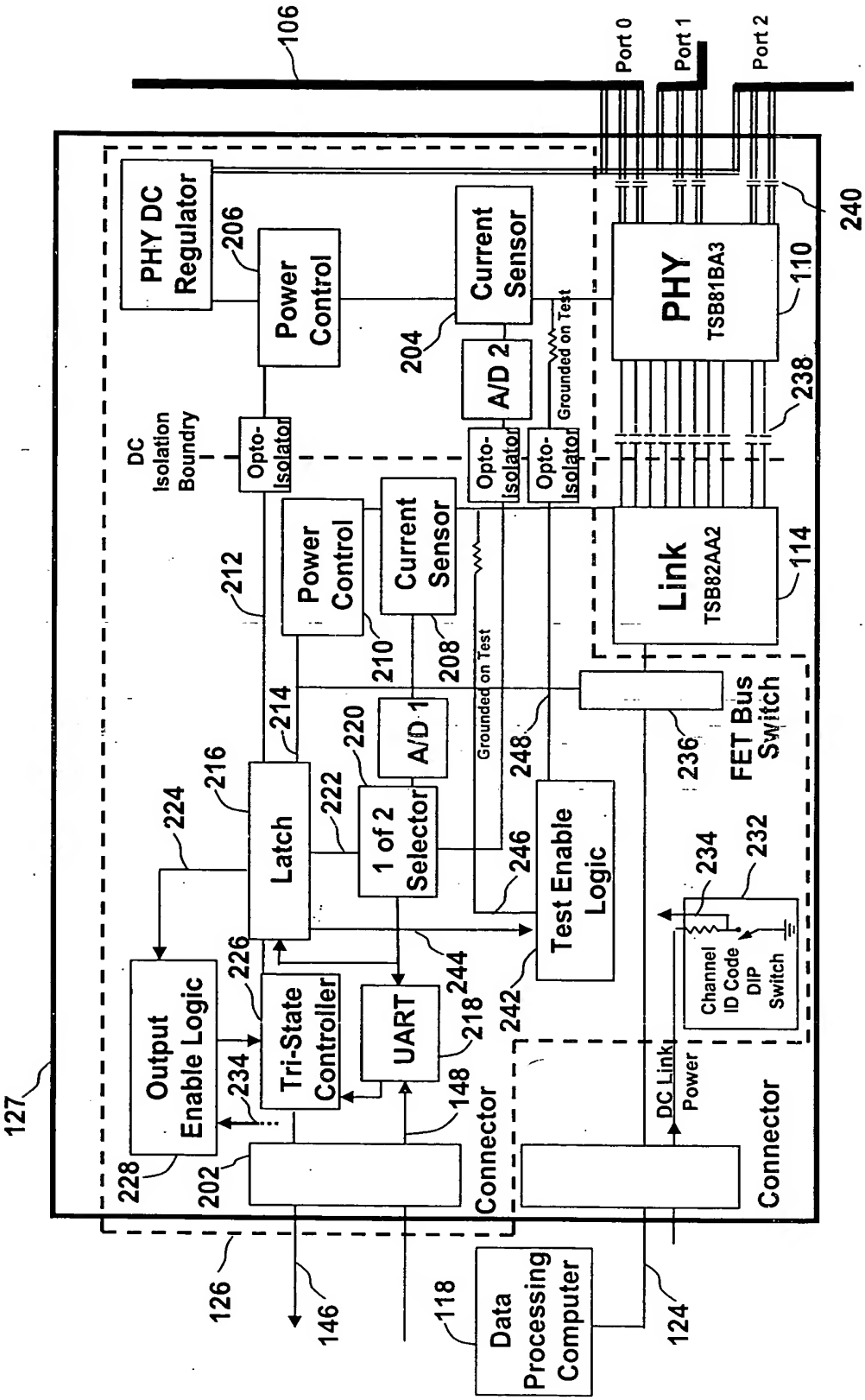

106
Port 0
Port 1
Port 2
240
PHY DC Regulator
206
Power Control
Current Sensor
204
A/D 2
Grounded on Test
PHY TSB81BA3
110
238
DC Isolation Boundry
Opto-Isolator
Opto-Isolator
Opto-Isolator
212
Power Control
Current Sensor
Link TSB82AA2
114
210
208
Grounded on Test
214
220
A/D 1
248
236
FET Bus Switch
216
224
Latch
222
1 of 2 Selector
246
Test Enable Logic
234
232
Channel ID Code DIP Switch
226
Output Enable Logic
Tri-State Controller
UART
244
218
242
234
148
DC Link Power
127
228
202
Connector
Connector
126
146
118
Data Processing Computer
124

FIG. 3

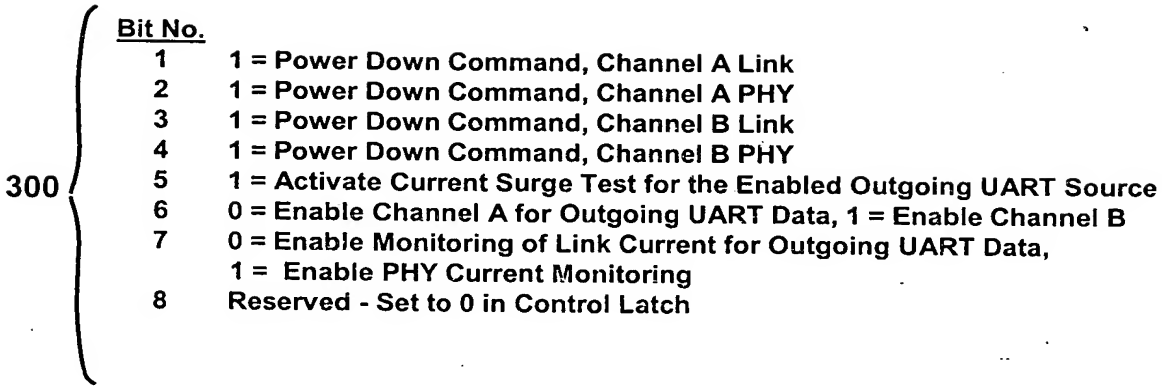

300
Bit No.
1 1 = Power Down Command, Channel A Link
2 1 = Power Down Command, Channel A PHY
3 1 = Power Down Command, Channel B Link
4 1 = Power Down Command, Channel B PHY
5 1 = Activate Current Surge Test for the Enabled Outgoing UART Source
6 0 = Enable Channel A for Outgoing UART Data, 1 = Enable Channel B
7 0 = Enable Monitoring of Link Current for Outgoing UART Data,
1 = Enable PHY Current Monitoring
8 Reserved - Set to 0 in Control Latch

FIG. 4

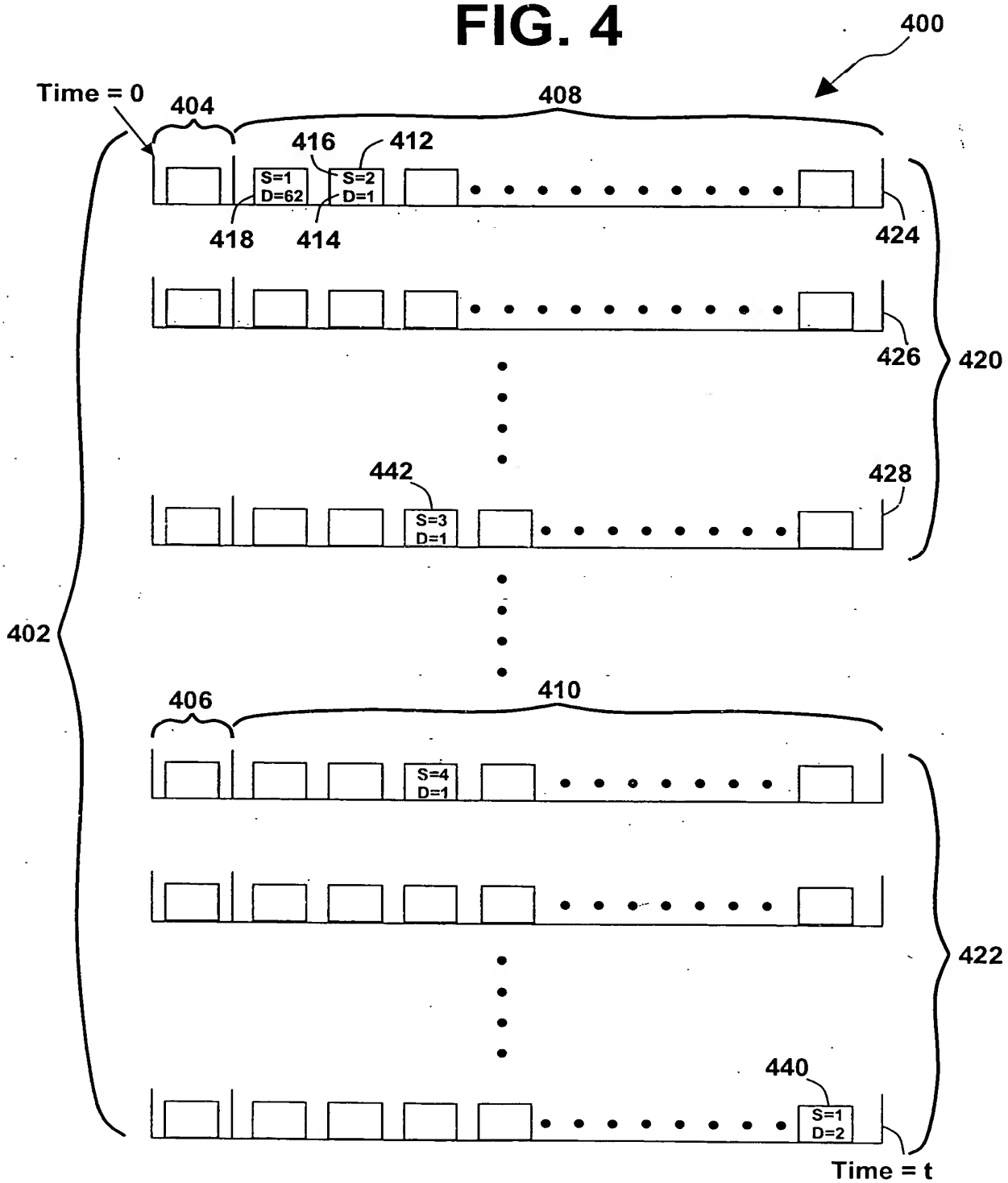

400
Time = 0
404
408
416
412
S=1
D=62
S=2
D=1
418
414
424
426
420
442
S=3
D=1
428
402
406
410
S=4
D=1
422
440
S=1
D=2
Time = t

FIG. 5

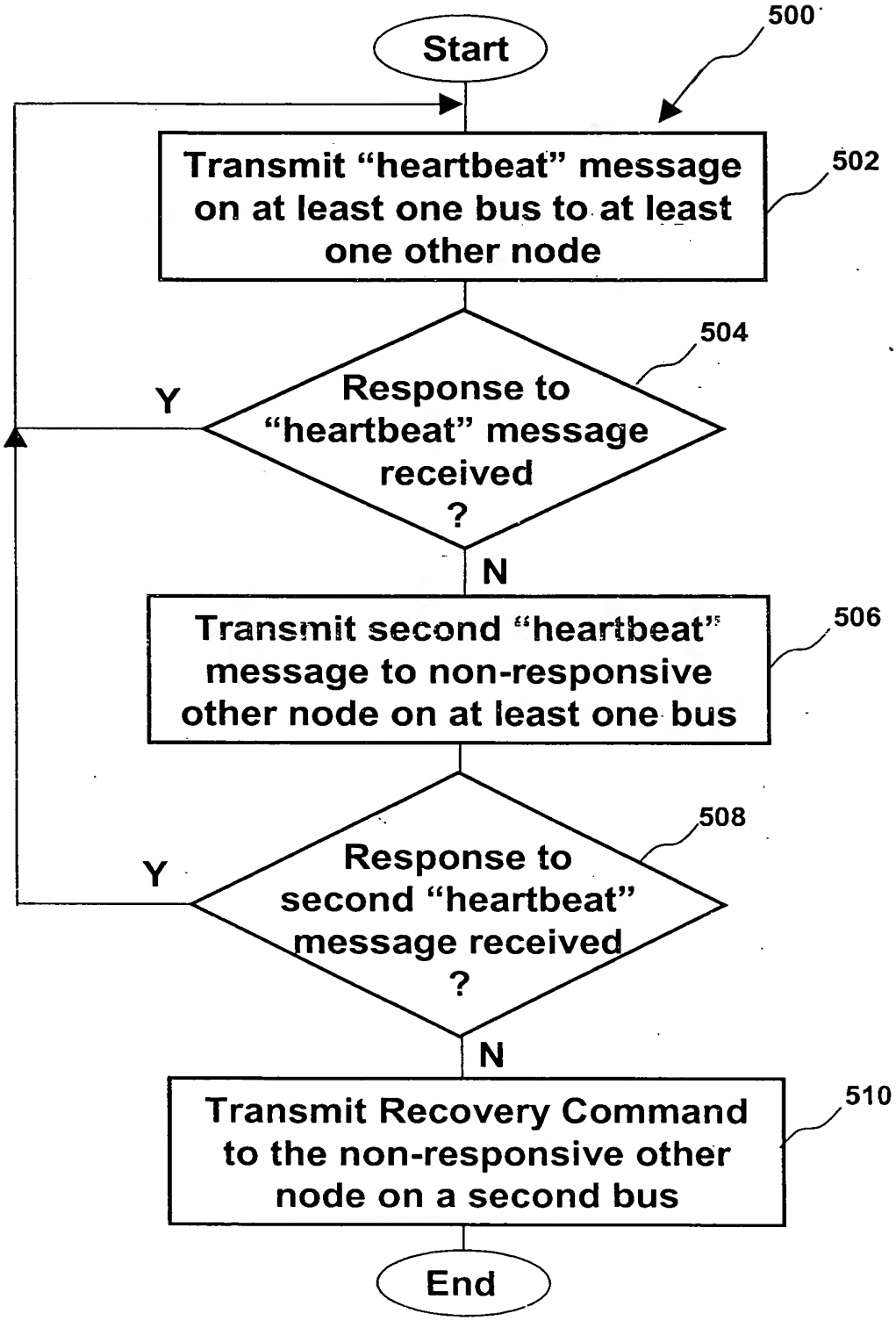

500
Start
Transmit "heartbeat" message on at least one bus to at least one other node
502
504
Response to "heartbeat" message received ?
Y
N
Transmit second "heartbeat" message to non-responsive other node on at least one bus
506
508
Response to second "heartbeat" message received ?
Y
N
Transmit Recovery Command to the non-responsive other node on a second bus
510
End

FIG. 6

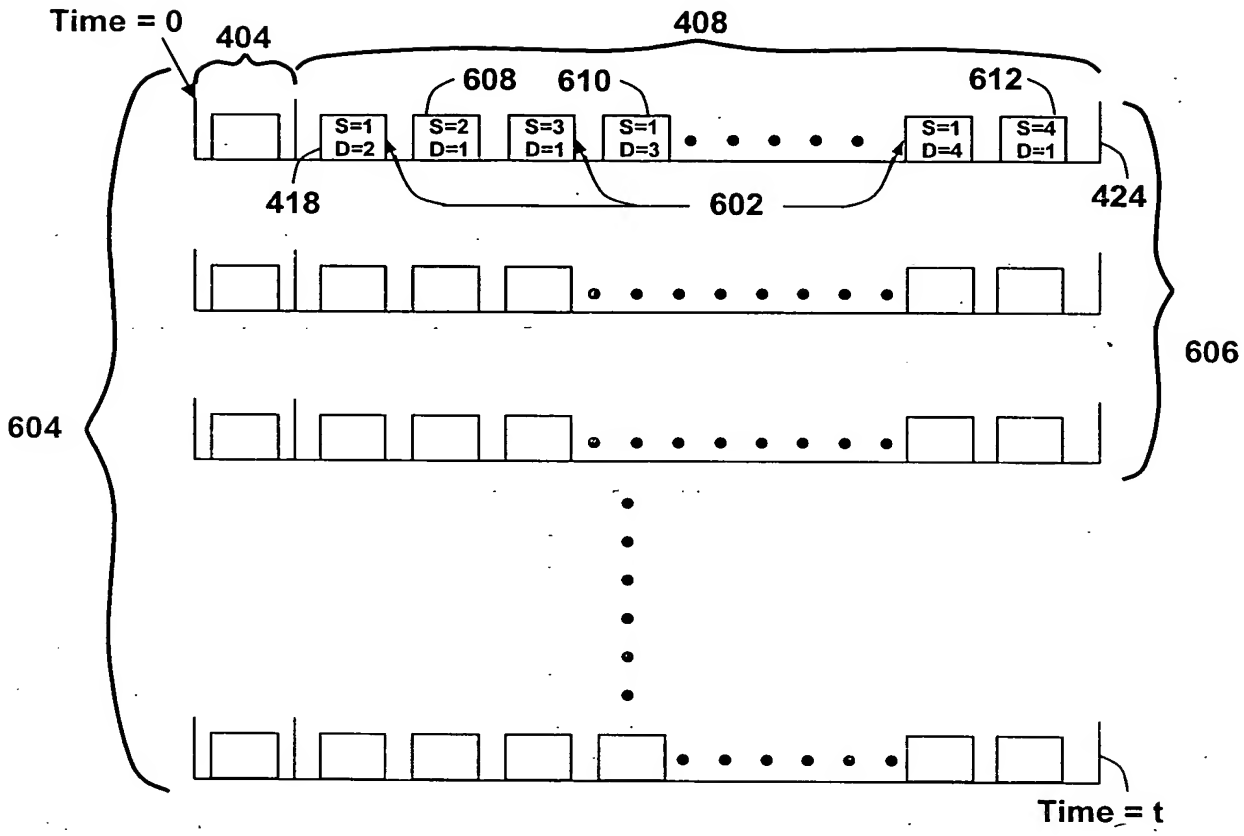

Time = 0
404
408
608
610
612
S=1
D=2
S=2
D=1
S=3
D=1
S=1
D=3
S=1
D=4
S=4
D=1
418
602
424
606
604
Time = t

FIG. 7

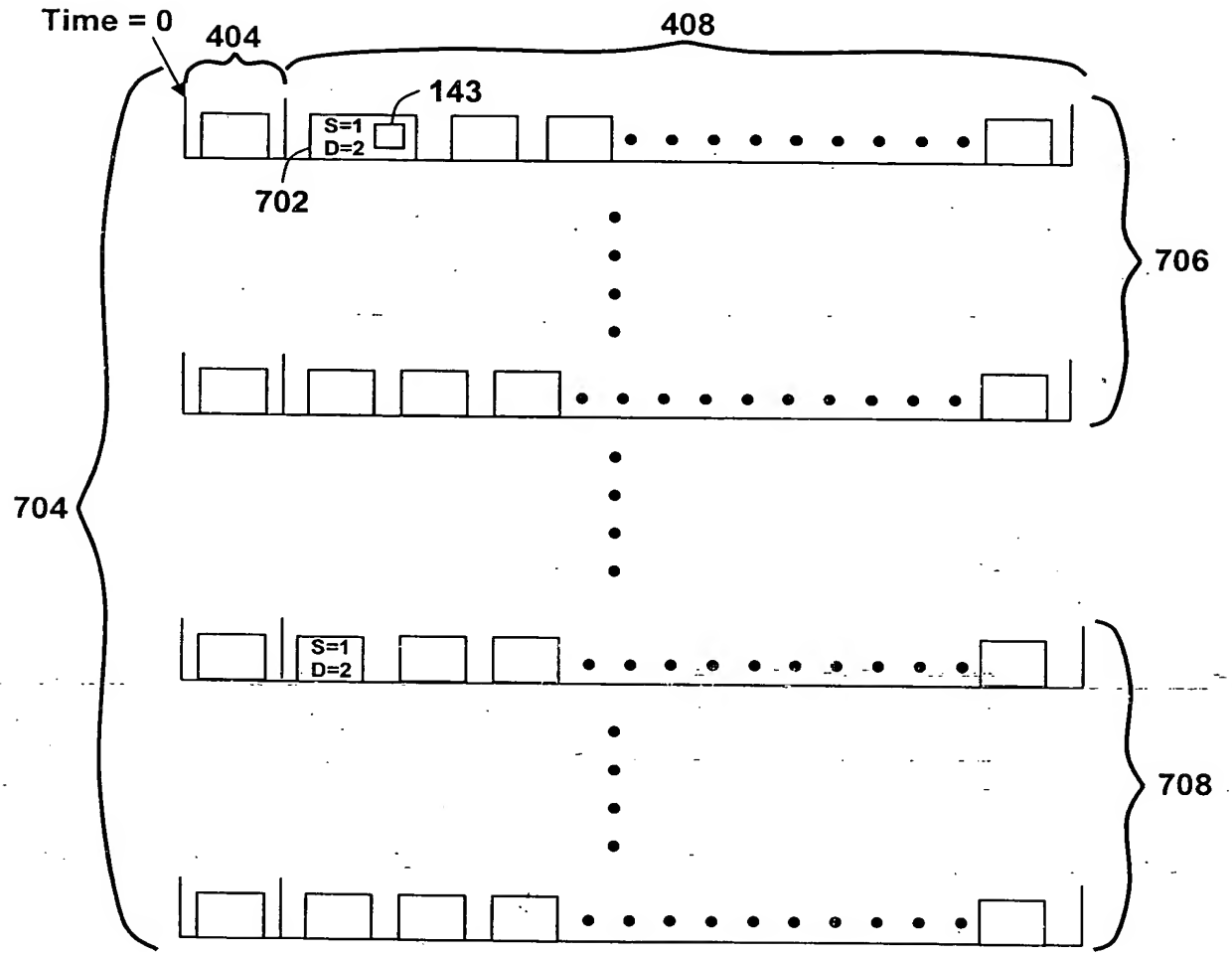


FIG. 8

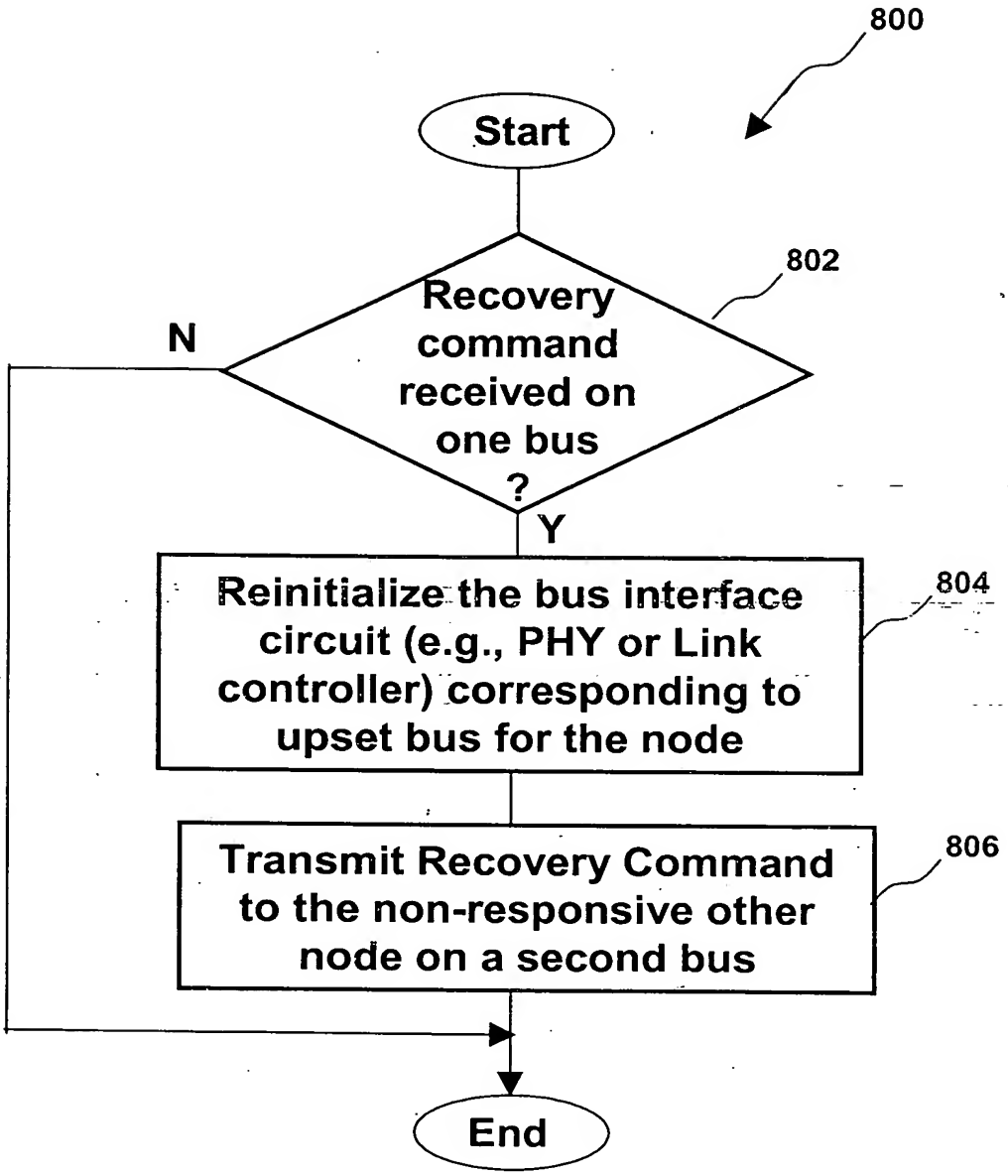

800
Start
802
Recovery command received on one bus ?
N
Y
Reinitialize the bus interface circuit (e.g., PHY or Link controller) corresponding to upset bus for the node
804
Transmit Recovery Command to the non-responsive other node on a second bus
806
End

FIG. 9

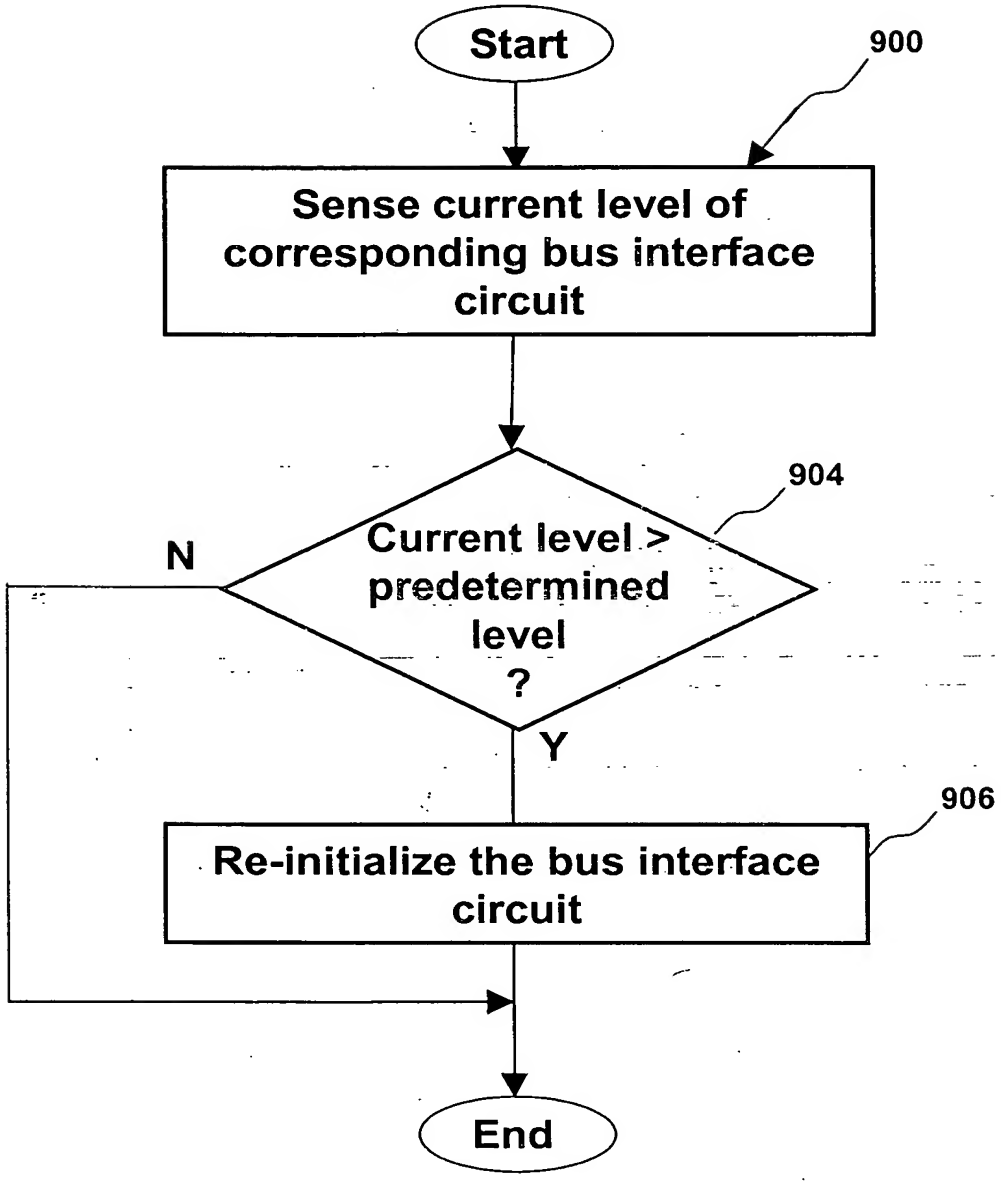

Start
900
Sense current level of corresponding bus interface circuit
904
Current level > predetermined level ?
N
Y
906
Re-initialize the bus interface circuit
End

FIG. 10

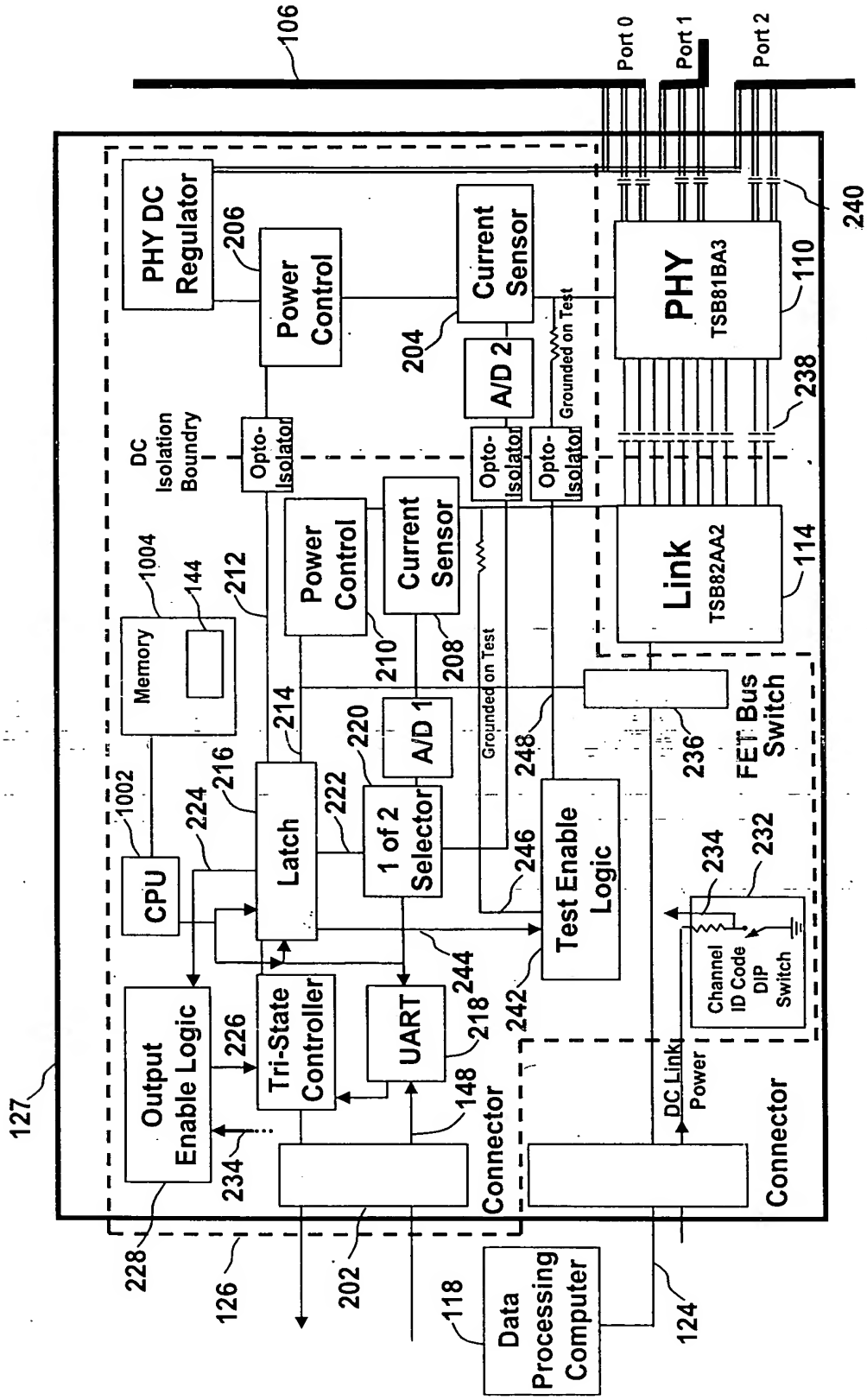
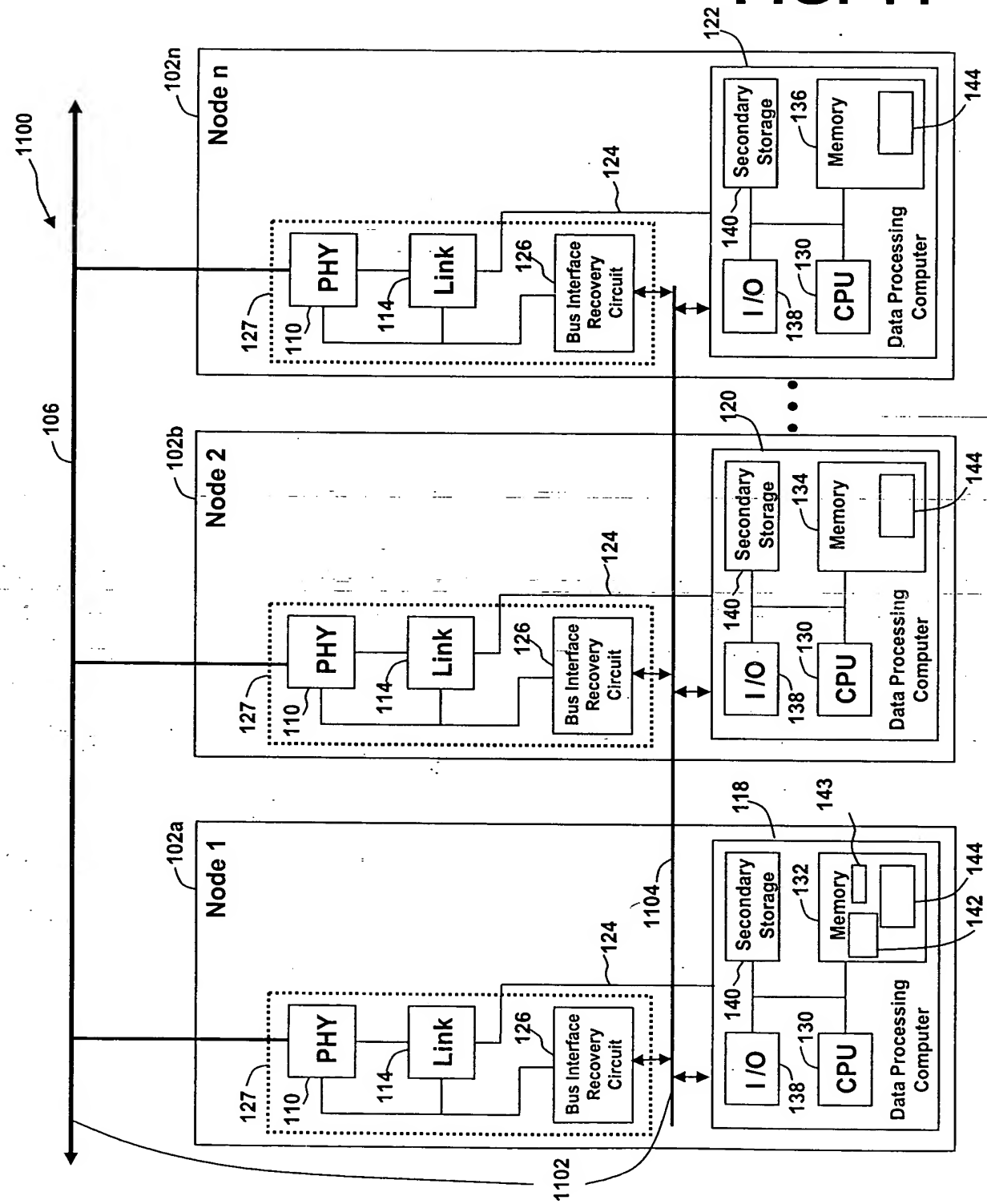

106
Port 0
Port 1
Port 2
240
PHY DC Regulator
206
Power Control
Current Sensor
204
A/D 2
Grounded on Test
PHY
TSB81BA3
110
238
DC Isolation Boundry
Opto-Isolator
Opto-Isolator
Opto-Isolator
Power Control
Current Sensor
Link
TSB82AA2
114
1004
144
212
Memory
210
208
214
220
A/D 1
Grounded on Test
248
236
FET Bus Switch
1002
224
216
222
Latch
1 of 2 Selector
246
Test Enable Logic
234
232
CPU
Channel ID Code DIP Switch
Output Enable Logic
226
Tri-State Controller
UART
218
244
242
127
148
Connector
DC Link
Power
Connector
228
126
202
118
Data Processing Computer
124

FIG. 11


1100
106
102n
Node n
102b
Node 2
102a
Node 1
1102
1104
PHY
Link
Bus Interface Recovery Circuit
Secondary Storage
Memory
I /O
CPU
Data Processing Computer
110
114
124
126
127
130
132
134
136
138
140
142
143
144
118
120
122